ABSTRACT

Disclosed herein is a synchronous SRAM-compatible memory and method of driving the same. The synchronous SRAM-compatible memory includes a DRAM array, a data input/output unit, an address input unit, a burst address generating unit, a state control unit, a refresh timer, and a refresh control unit. The data input/output unit controls input and output of data. The address input unit inputs a row address and a column address. The burst address generating unit generates a sequentially varying burst address. The state control unit generates a burst enable signal that enables the burst address generating unit, controls the data input/output unit, and generates a wait indication signal while an access operation of a previous frame is performed with respect to the memory array. The refresh timer generates a refresh request signal activated at regular intervals. The refresh control unit controls the refresh operation with respect to the DRAM array in response to the refresh request signal.